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Novel Technique for Utilizing Analogue Video Signal for IRFPA Raw Data Transfer for Calibration Purposes

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Authors' contributions

This work was carried out in collaboration between both authors. Author AMA designed the study, performed the statistical analysis and wrote the first draft of the manuscript. Author AAAA managed the analyses of the study. Author AMA managed the literature searches. Authors AAAA and AMA wrote and developed the protocol. Both authors read and approved the final manuscript.

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Abstract

Infrared focal plane array (IRFPA) is a bi-dimensional array of micro scaled infrared detectors which become essential sensing devices in a wide range of applications. Due to the need for mobility and power saving, new uncooled IRFPA's have become more suitable to substitute cooled IRFPA in many applications that require lighter weight and lower power consumption. Electronic Designers aim to reduce power consumption by integrating circuits inside high-density chips, invent new solid state components which consume less power and eliminate excess components when they are rare to use. This paper focuses on eliminating high speed digital data link channel from low profile portable IR camera and instead of that, it proposes manipulating bit arrangements by video processing unit to overcome video signal major issues like noise, clipping, and pixel resolution.

Keywords: IRFPA; uncooled thermal camera; calibration; TPC; FPGA; Verilog; LabVIEW; composite video; DAC; GigE; white level clipping; low power consumption.

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1 Introduction

Infrared focal plane array (IRFPA) is a two dimensions matrix of micro infrared detectors which collect photons on a certain wavelength [1]. In most of the literatures, they call it infrared detector although it is constructed of rows of micro detectors. Either alone or combined with others, IRFPA becomes an essential sensing elements in a wide range of applications like robotics, medical, military, astronomy and surveillance [2]. Due to the nature of IRFPA sensing which could represent a new dimension of physical image that cannot be seen by naked human eye [3]; researchers have spent years of effort to develop this type of a sensing device starting from one propping detector to a bi-dimensional matrix which can be easily represented as an image showing a heat distribution map (image) for a targeted body [4]. Besides that, IRFPA's types have developed from cooling dependent detectors to have a very competitive uncooled IRFPA. Although both types have their own specific scope of use which still in use, and their demands, which are growing, but the need for mobility guided the need to develop uncooled IRFPA closer to cooled IRFPA in the matter of image resolution and micro detector size [5].

Mobility forces any electronic device to be less in power consumption, size and weight. Besides eliminating the cooling engine, as in cooled IRFPA, which is the most power consuming part; modern uncooled IRFPA is aiming to hardwire as much as possible of readout circuitry elements on micro based footage inside the IRFPA detector to eliminate power dissipations. According to this concept, designers are challenged to circuits and invent techniques to satisfy requirements with less electronic components.

This research aims to eliminate the need for using a high speed digital channel to transmit image data and focuses on developing a reliable low cost technique to utilize composite video signals as data carries for IRPFA calibration process.

2 Background

Unless implementing an external ADC unit; modern uncooled detectors are internally equipped with 12 bits ADC within a complete set of hardwired pre amplification components and analogue conversion to a digital unit. Fig. 1 illustrates the whole block diagram related to the interest of research in this paper. Also, Fig. 1 shows the ideal design when the pre amplification circuit is separated from the detector although modern detectors give the flexibility to utilize the internal pre amplification circuit.

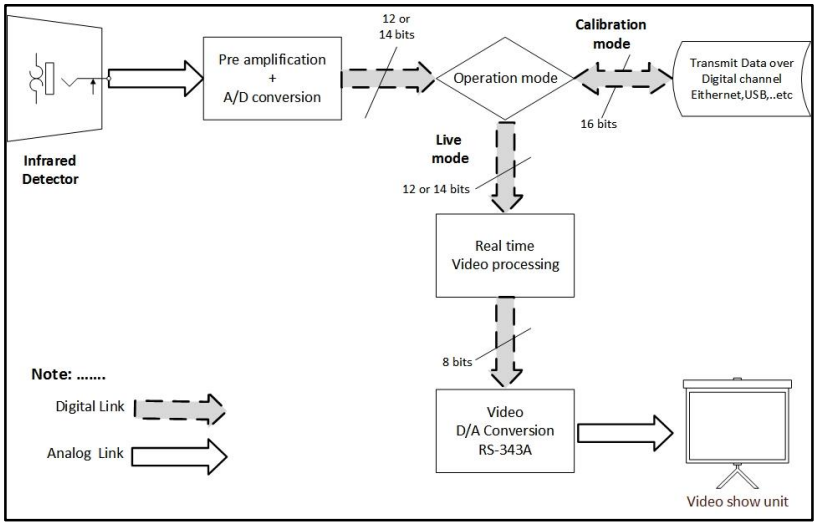

Fig. 1. System basic operation modes

This research made on a detector who gives a 12 bit raw data but it is capable to integrate with external 14 bit ADC, too. The research is to save more power by finding out a solution towards eliminating more components; researchers in this paper build their proposed technique upon utilizing the internal integrated circuit.

When the system operator selects to work on live mode, the raw data stream shall be processed by a real time video processing unit to correct the image and to do some needed image enhancements before it is made ready for presentation. By its nature, infrared detector creates mono color image which needs 8 bits gray scale representation, only. To do so, a resolution reduction task shall be implemented in the last stage of real time processing to convert the data from 12 to 8 bits type which shall be suitable for wide range of video show devices. Fig. 2 illustrates video DAC clocking diagram which is capable for RGB video streaming, also. In case of mono color as in IRFPA, a designer can select any of 8 bits channel and short remaining two channels to ground to assure zero level.

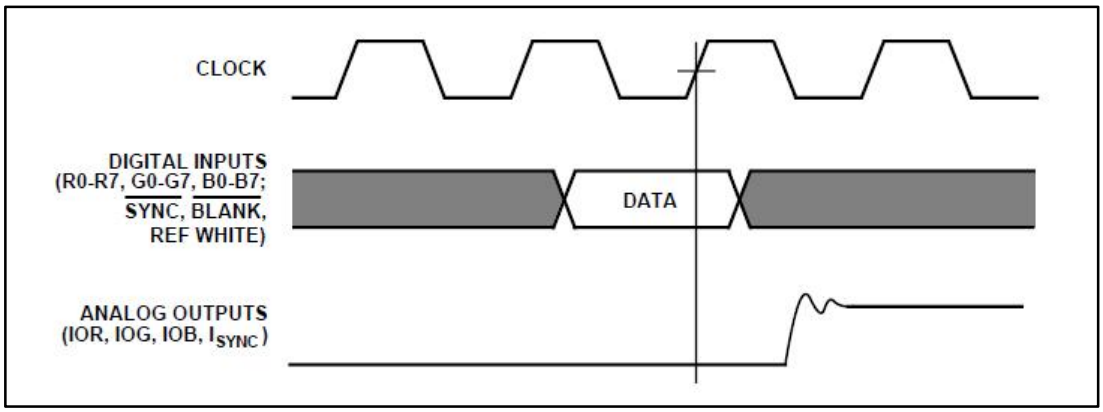

Fig. 2. Video DAC clocking diagram

Calibration process is the task to take the system to a standardized platform to read and reset the system under ideal conditions [6]. This task needs to process raw data streams without any image enhancement process. Raw data shall be in a form of 8 bits or multiples to match the need to perform software operations on the data. Due to the need for 12 bits or higher ADC resolution, a 16 bits data packet is enough to carry a single pixel data. In order to have a reliable calibration data, modern systems are equipped with at least one high speed digital channel either for purpose of gathering the raw data or presenting the video using embedded system.

IRFPA Calibration process is a very slow process and requires a prepared lab for purpose of IRFPA calibration routine which normally has to have optical bench, blackbody and frame grabbing system. One of the most popular and efficient IRFPA calibration techniques is to calibrate for two point correction purpose (TPC) which corrects non-uniformity phenomena in micro detectors response for similar referenced source in front of all of them [7] [8]. TPC relies on first order approximation for non-uniformity behavior over a range of temperature:

$$y_{ij}(k) = a_{ij}(k)x_{ij}(k) + b_{ij}(k) \quad (1)$$

Where

(ij) is micro detector (or pixel) address in the array.
; k is frame sequence
; y_{ij} is the pixel response
; x_{ij} is actual radiation

The purpose of TPC is to find out the gain and offset from a sequence of temperature measures. Correcting gain and offset shall strip fixed pattern noise and temporal noise which are added naturally due to manufacturing tolerance and purity of core material [9]. From equation 1;

$$G_{ij} = \frac{1}{a_{ij}} \tag{2}$$

$$O_{ij} = \frac{b_{ij}}{aij} \tag{3}$$

Where G_{ij} is the gain value for a pixel and O_{ij} is the offset value for the same pixel so that

$$x_{ij} = G_{ij} y_{ij} - O_{ij} \tag{4}$$

Digital calibration channel offers a very reliable carrier due to full duplex feature which both sides communicate while transmission to assure a correct receiving beside over heading the data by check sum and some extracted information to check received data quality and minimizing data rejection. Most of calibration routines suggest gathering a multiple of 16 frames to create one averaged frame under that moment of calibration process which requires consecutive farms. For this reason, the system shall has a high speed digital channel and avoid using RS232 channel although it is available in most systems.

Digital channel has the task to carry back an updated lookup tables which holds new calibration data. This stage of calibration process which would normally being the final step does not require a speedy carrier and could transfer data on a slower digital channel.

3 Analogue Video Characteristics

Video signal carries video information to video show device which is a manipulated data of original raw data but after correction, image enhancement and range reduction from 12 to 8 bits.

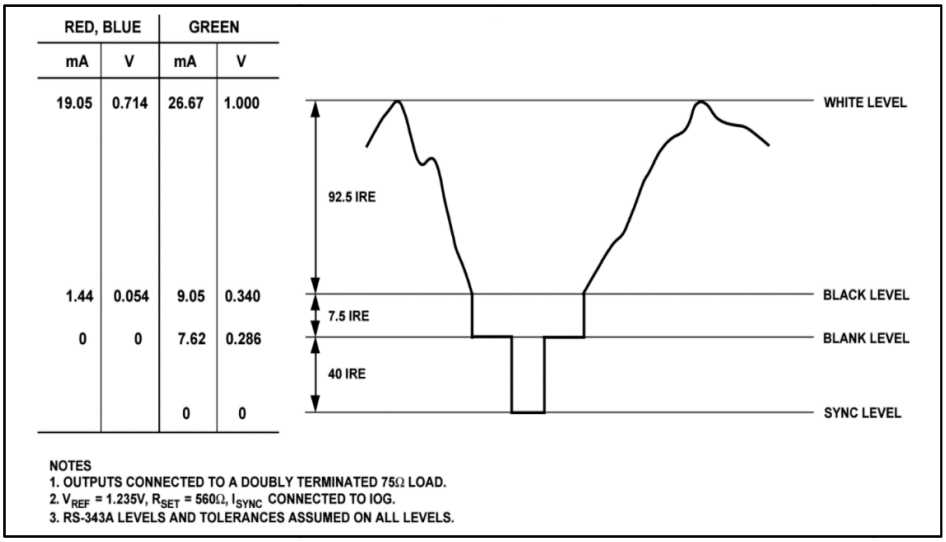

Fig. 3. Video signal output waveform

There are three challenges while using video signal as a data carrier. First, video signal is an open_loop analogue signal which links in one way direction starting from a transmitter to a listening receiver without

any kind of feedback. Video signals has a coded signal which trigger for beginnings of frames and lines. Second, RS-343 support 8 bits gray scale representation which is not enough for higher dynamic ranges like 12 bits in this topic. The third reason is that video signal tolerates highly in a matter of signal quality because at the end, it will represent the gray level as a change in voltage level which needs serious rules to avoid issues of early clipping, noise and impedance mismatching. Some of the issues could be controlled on design rules level like impedance matching [10].

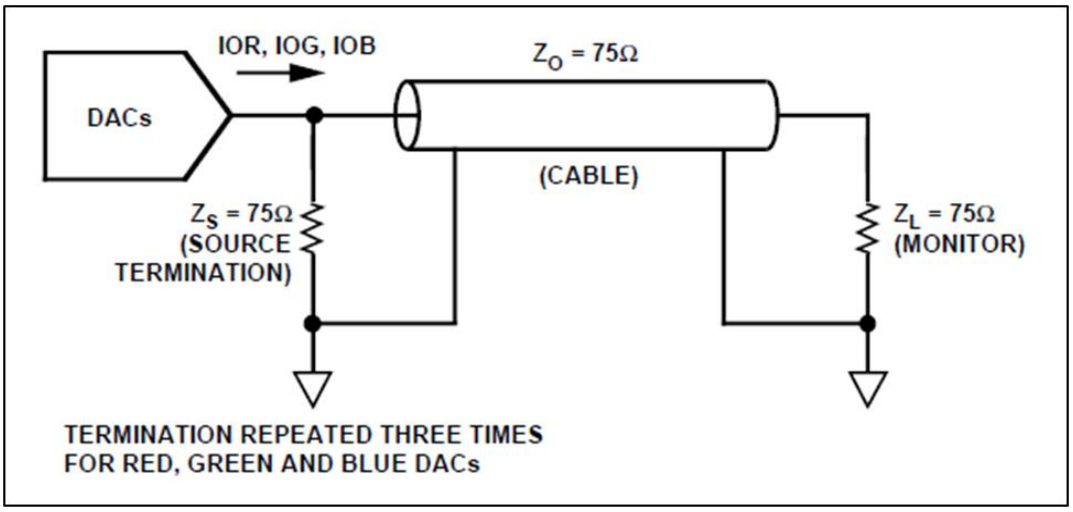

Fig. 4. Impedance matching design guide for analogue video

Mismatching is an issue that could seriously reduce the final aggregated power at receiver or increasing the noise figure. Matching the impedance requires a proper termination which following rules [11] as in Fig. 4. Fig. 4 considers a well matching design after video DAC output in transmitting side and before video ADC input in receiving side; including circuit design and the selection of video connecter e.g. BNC type as well. This has nothing to do with cable except to assure selecting a high quality cable with the same impedance matching, as well.

4 Proposed Technique

During continuous applied research and studies on thermal imager based on IRPFA form model rearches could find three major limitations that have to be solved before utilizing video signal for transfering 12 bits raw data for calbration purpes.

1. Most video DAC's support 8 bits digital data input for gray scale level or 8 bits three channels RGB which means that data shall be split into two 8 bits packets.
2. Due to extreme testing with different DAC's in transmission and receiving to assure receiving any data correctly within packet range from 0 to 255 decimal; researchers found out rare cases of level clipping below but close 255 decimal level which means there is a risk of not reaching or reading the maximum voltage level which means the maximum packet value shall be considered to not be reaching a certain threshold.
3. An influence by noise affects the minimum digital resolution. It could change the gray level few grades higher or lower. Noise affect can be a serious issue in the most significant packet due to a packet merge operation that shall be done in the destination to gather back the desired 12 bits raw data. There for, merging incorrect (noisy) packet in the most significate side shall extremely offset the data.

A Proposed technique could solve all issues by implementing new procedures in transmitting and receiving sides when the operator changes the system mod as in Fig. 1 to calibration mode.

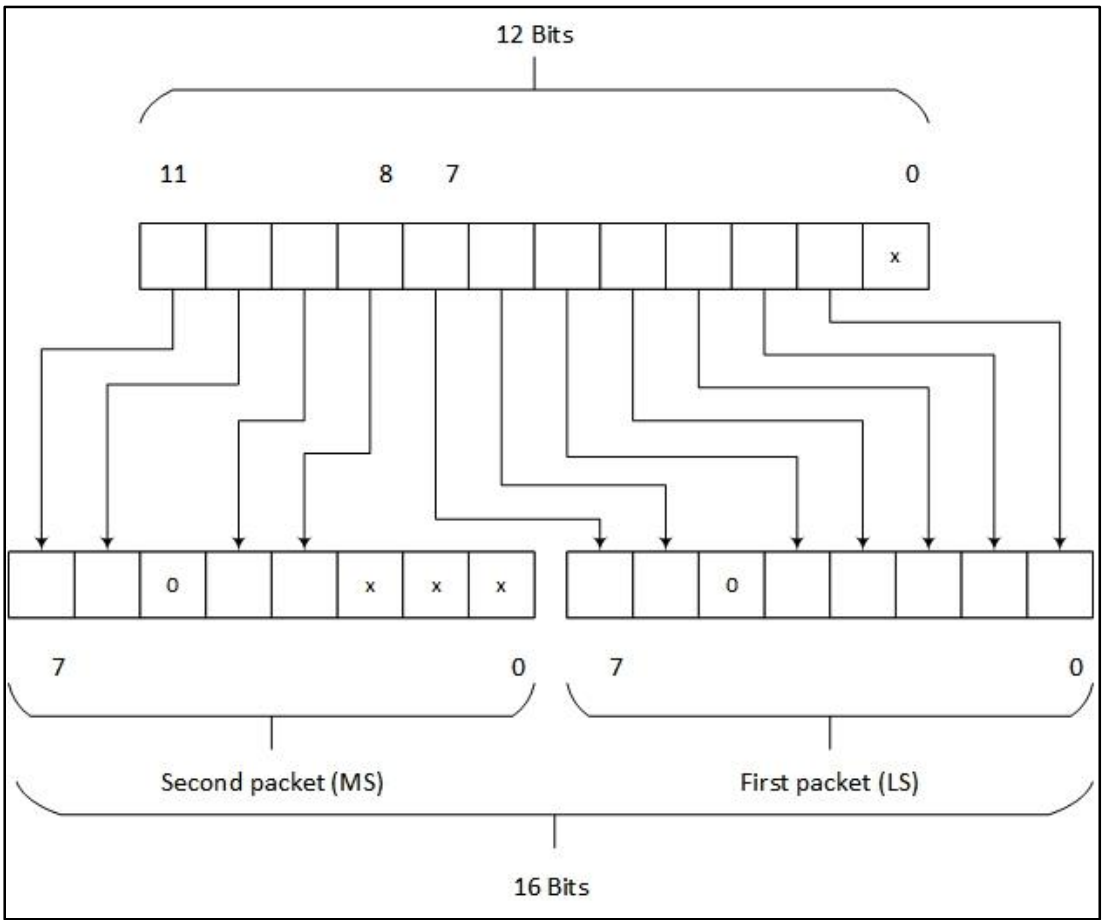

Fig. 5. Two packets data manipulation

Fig. 5 demonstrates bits distribution among packets. Bit0 is the least significant bit and which has a minimal impact on data value because its value change as a matter of error is 1/16 of the error impact in case of convergence to 8 bit data streaming for real-time operation mode. In real time operation mode which is 8 bit grayscale representation; will not observe any effect if the gray level was changed by one level more or less which practically means neglecting the value of the least significant bit or (bit 0). Saving the position of bit 0 of the 12 bits raw date will enhance the reliability to receive more stable data.

Bit 5 in both packets represents the value of 32 decimal. Among testing the maximum value sent and received over video line which should be 255 the research found that in rare cases it was received in a less amount because the analogue level was clipped earlier than the desired level. Also, cable quality and impedance matching and filtering circuit affects the level of the signal which will represent in different but a close value. Fixing bit 5 of all of the packets, while steaming to the value 0, basically means to avoid the maxim value of reaching more than 233 decimal in any packet which keeps the interpolation to analogue signal by video DAC in a very safe place of clipping.

Out of the remaining 11 bits data resolution after ignoring bit 0, first packet will carry 7 bits of according to bit distribution in Fig. 1. Any noise level may interrupts an analogue signal that will appear as fluctuation on the least part of digital value which will increase the minimum resolution value. This paper proposes that the calibration process shall be done in a restricted lab which uses reliable tools and cables to minimize the influence on calibration process. And as a reliability assurance, the proposed technic bypasses the three least significant bits of second packet. The receiving side has to combine both packets to one 12 bits packet. Any impact of noise level on the second packet which will appear as a tiny change in the least significant part of the second packet shall appears as a high fluctuation impact on the 12 merged bits. This is due to a significate change in bits position e.g. (bit 0 in the second packet shall be bit 8 in 12 bit merged packet). This situation presents a serious issue of reliability which guided the technic to position the remaining 4 bits of 12 bits raw data in a place far away of noise impact as in Fig. 5.

5 Experiment and Results

Instead of using high speed digital like for calibration purposes, researchers utilize a video frames grabber to collect and digitize frames for calibration device. Fig. 6 demonstrates the experiment setup. Instead of calibration digital link as in Fig. 1, the setup shall use the analogue link which used for carrying video to video-show device (see Fig. 1) to carry calibration data to calibration PC. A video grabber in between shall condition the video signal and digitize it into bit form.

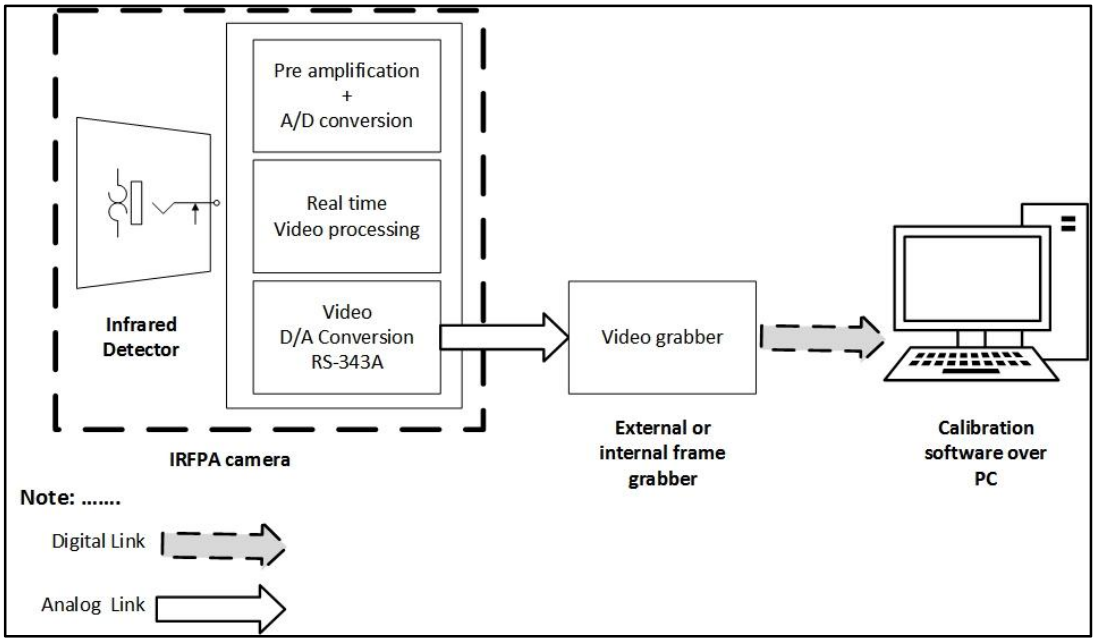

Fig. 6. Experiment setup which consists of IRFPA camera, calibration PC, and video frames grabber in between

Real Experiment setup as in Fig. 7 uses a video grabber from Pelora (product: iPORT analog-Pro External Frame Grabbers). This video grabber can collect pixels and digitize them and send them through GigE channel to calibration PC. IRFPA camera has a Ulis detector (model UL 03 26 2 size 384x288) and is equipped with UART link (RS232) to the processing unit whom researchers could utilize it for operations command & control and to update correction lookup tables due to analogue video channel is one direction channel. Fig. 8 shows closer view for IRFPA Camera, optics and video grabber.

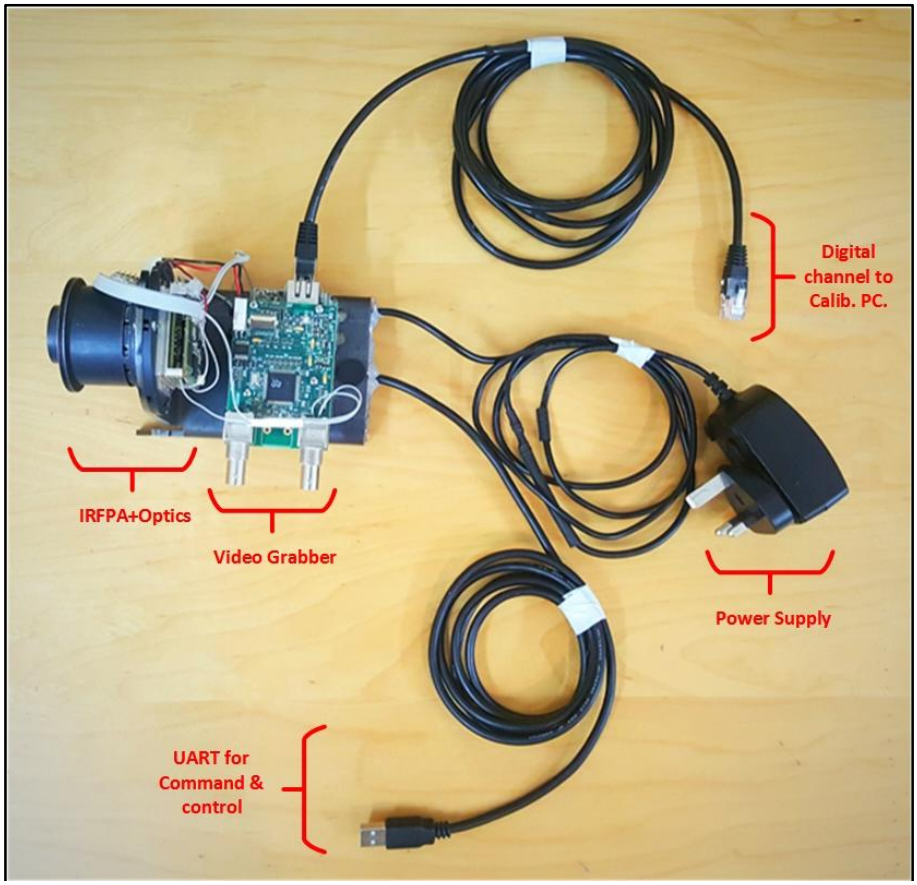

Fig. 7. Experiment setup

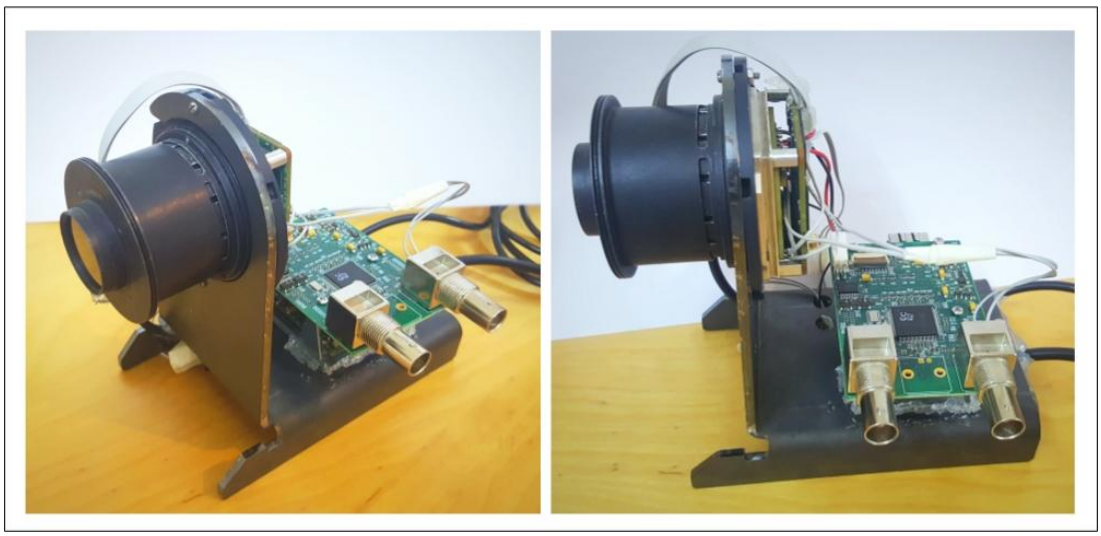

Fig. 8. Setup closer view

Video driving circuit which is a part of camera electronics designed with consideration for a 75Ω impedance matching. Moreover, Fig. 9 shows an OpAmp which is in purpose for eliminating power decay issues that caused by long transmission cables.

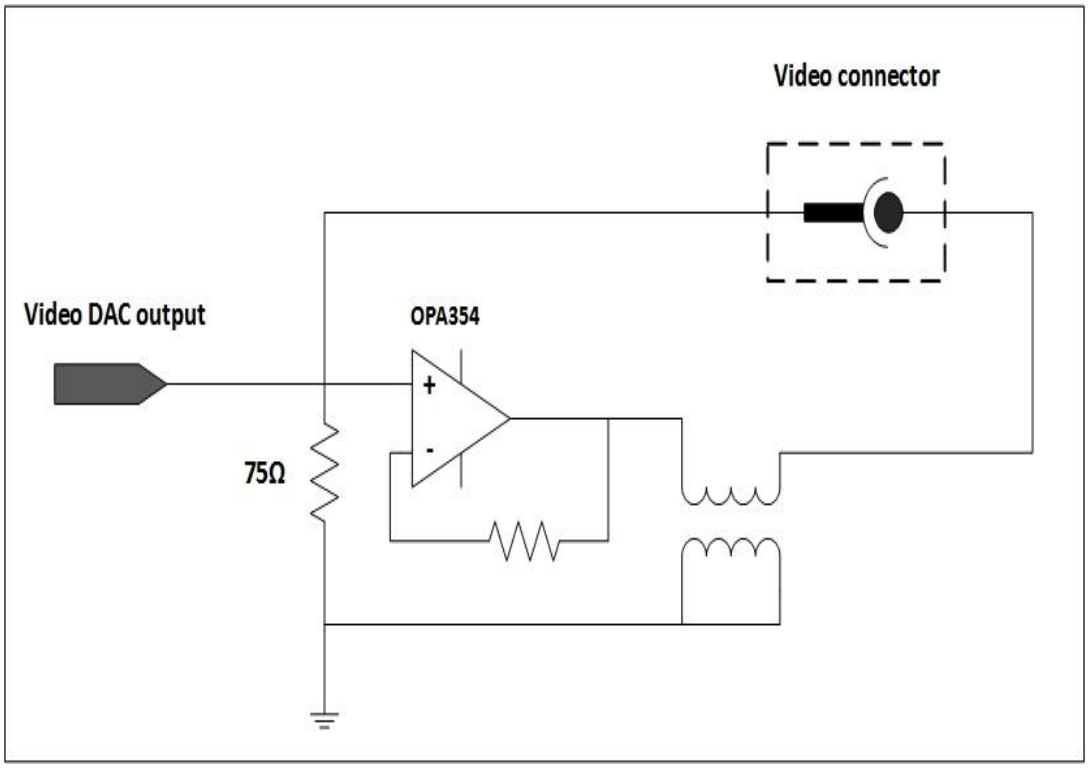

Fig. 9. Impedance matching circuit

Regarding Fig. 5, researchers redesign video processing FPGA to handle two packets requirements. Fig. 10 illustrates processes and parallel modules modifications. In this research we suggest two 8 bits FIFO's to handle the two packets where the first FIFO shall handle lower significant packet and second one for most significant packet. Verilog code has to generate a new clocking system and create new parallel modules for the new transmission schema.

```
//============================================================
PLL_IP_Module(
   .POWERDOWN              (1),
   .CLKA                   (clk_24_5_MHz),
   .LOCK                   (CLK_OK),
   .GLA                    (CLK_59MHz),
   .GLB                    (CLK_14_75MHz),
   .GLC                    (CLK_7_375MHz)
   );
//============================================================
```

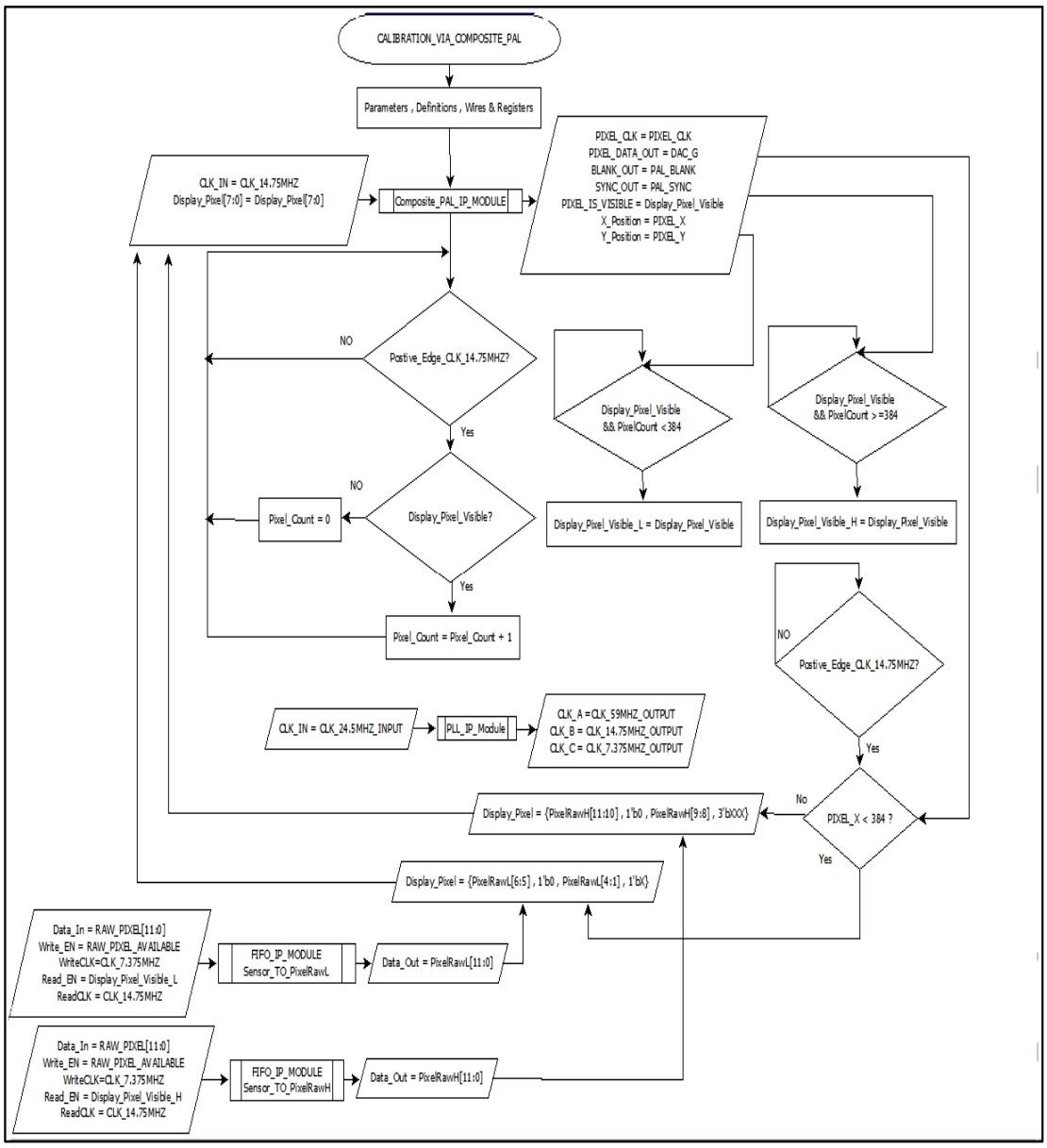

Fig. 10. FPGA reconfiguration for two packets arrangement

To align with analogue video clocking rules and due to frame grabber limitations by the manufacturer; FPGA has to send first FIFO data and hold the second FIFO until the end of all real pixels before it starts sending the second FIFO data.

```
//============================================================

   assign    Display_Pixel_Visible_L   =   Display_Pixel_Visible && (Pixel_Count < 384) ;
   assign    Display_Pixel_Visible_H   =   Display_Pixel_Visible && (Pixel_Count >= 384) ;
//============================================================
```

```
always @(posedge CLK_14_75MHz_PLL or negedge S_rst )begin
            if(!S_rst) begin
        Pixel_Count  <= 0;
    end else begin
        if(Display_Pixel_Visible) begin
            Pixel_Count  <= Pixel_Count + 1;
        end else begin
            Pixel_Count  <= 0;
        end
    end
 end
//============================================================
always @(posedge CLK_14_75MHz_PLL or negedge S_rst )begin
            if(!S_rst) begin

    end else begin
        if (PIXEL_X_X<384)Display_Pixel = {PixelRawL[6:5],1'b0,PixelRawL[4:1],1'bX};
        else Display_Pixel = {PixelRawH[11:10],1'b0,PixelRawL[9:8],3'bXXX};
        end
end
//============================================================
```

On calibration PC, researchers developed a software based on LabVIEW platform to aggregate data from GigE port and reconstruct the 12 bits data recursively, according to Fig. 5.

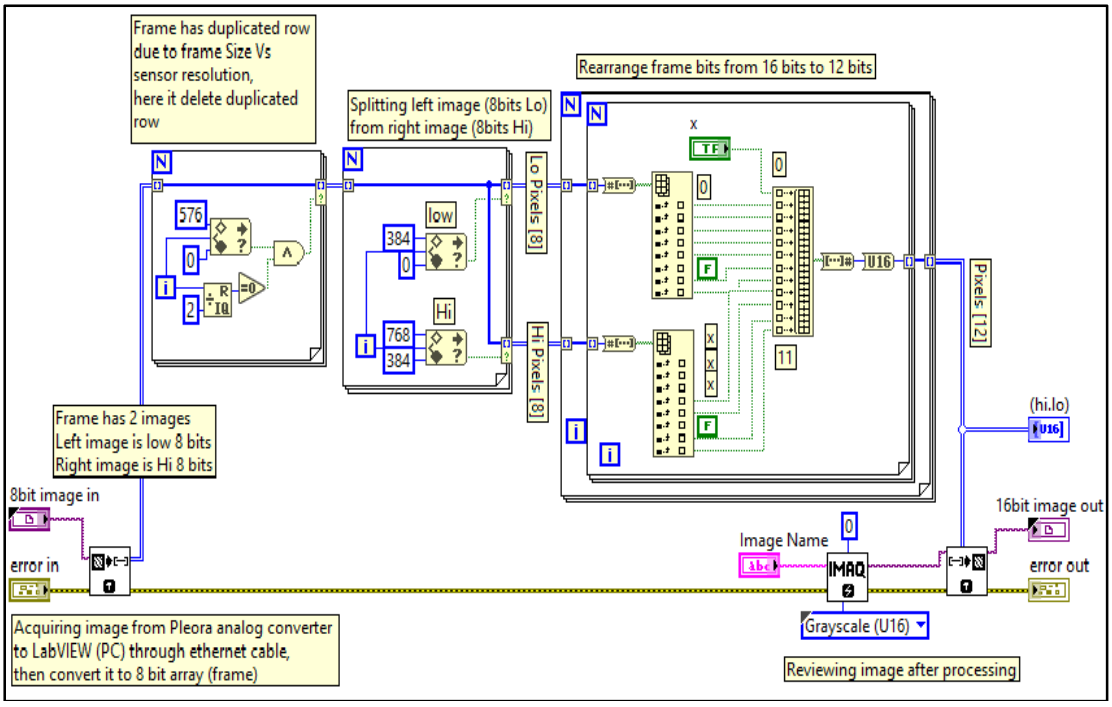

Fig. 11. LabVIEW sub VI's for data aggregations and bit mapping to 12 bits original form

Fig. 11 shows part of calibration software where to collect data from GigE buffer [12]. It shall capsulate pixels in 16 bits forms to be suitable for video processing purposes over PC; by set all upper four bits to zero.

Resulting from this research's promising technique, it resolves the most challenging obstacles to utilize video signal for 12 bits or higher data transmission.

6 Conclusion

This research could solve the need to save more power and space by eliminating rarely used electronics and instead of that, it proposes utilizing video channel for calibration purposes. Composite video standard could satisfy carrying 384x288 pixels but in higher resolutions may need more efforts to customize frame video grabber for this purpose.

7 Future Work

As this paper could eliminate the need for high speed digital channel like GigE or others, but it eliminates the feature of networking and security, also. In Most cases, IRFPA is calibrated as a pair-to-pair communication where this research fits well; but due to wide range of use for IRFPA, it could be better to add networking and security features [13] to communicate many (IRFPA systems) to one (remote calibration center) to do and archive fast calibrations. In case of wireless intermediate, network life time shall be an issue during data transmission and needs serious consideration [14].

Competing Interests

Authors have declared that no competing interests exist.

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